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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/568,961	02/22/2006	Mitsuyoshi Mori	0719710423	8584
53080 7590 09/03/2008 MCDERMOTT WILL & EMERY LLP 600 13TH STREET, NW WASHINGTON, DC 20005-3096				
EXAMINER				
PATEL, REEMA				
ART UNIT		PAPER NUMBER		
2812				
MAIL DATE		DELIVERY MODE		
09/03/2008		PAPER		

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/568,961

Applicant(s)

MORI ET AL.

Examiner

REEMA PATEL

Art Unit

2812

Period for Reply -- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 July 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 63-70 and 72-92 is/are pending in the application.
- 4a) Of the above claim(s) 63-69, 72-76, 78-80, 82 and 84-86 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 70, 77, 81, 83 and 87-92 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 22 February 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-849)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 7/17/08 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 70, 77, 83, and 88-92 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue et al. (U.S. 2003/0127667 A1; hereinafter 'Inoue') in view of Houston (U.S. 6,096,612).

4. Regarding claims 70, 77, and 83, Inoue discloses a solid state imaging device, for use in a camera device ([0002]), in which a plurality of unit pixels are arranged on a substrate, each unit pixel including a plurality of element formation regions (32, Fig. 1) and element isolation regions (36, Fig. 1) between the element formation regions ([0007]-[0008]). Inoue discloses that the element isolation regions comprise of trenches ([0007]) but does not disclose the specific steps (a)-(e) in

forming the trench isolation regions and hence does not disclose forming the photoelectric conversion section and an active region in the element formation regions after the step (e) in a step (f).

5. However, Houston discloses forming a trench by the following steps:

- A step (a) of forming, on the semiconductor substrate (12, Fig. 1), a protection film (16, Fig. 1) including an opening portion that exposes the element isolation formation region and a region located beside the element isolation formation region of an upper face of the semiconductor substrate (col 5, lines 35-50);
- A step (b) of forming a sidewall (24, Fig. 3) on a side face of the opening in the protection film (col 5, line 51 – col 6, line 6);
- A step (c) of forming a trench (26, Fig. 4) in the element isolation formation region in the semiconductor substrate by etching using the protection film and the sidewall as a mask (col 6, lines 7-13);
- A step (d) of oxidizing a side face portion of the trench in the semiconductor substrate by using the protection film and the sidewall as a mask after the step (c) to form an inner wall thermal oxide film (64, Fig. 10) (col 7, line 54 – col 8, line 2);
- A step (e) of forming an element isolation region by burying the trench with a burying film (74, Fig. 12) after the step (d) (col 8, lines 25-30);

6. Houston further discloses that the inner wall thermal oxide film is formed to an edge of the semiconductor substrate which is located at an upper edge portion of the trench (Fig. 10).

7. Because both Inoue and Houston teach methods to form isolation regions, it would have been obvious to one skill in the art at the time the invention was made to substitute one method for the other to achieve the predictable result of forming an isolation region between active components in a semiconductor device.

8. Regarding a step (f) of forming a photoelectric conversion section and an active region in the element formation regions after the step (e), Inoue discloses forming a photoelectric conversion section and an active region in the element formation regions ([0008]) but does not specifically disclose that it is after a step (e). However, it would have been obvious to one of ordinary skill in the art at the time of the invention to form the photoelectric conversion section and an active region in the element formation regions after forming an element isolation region because selection of any order of performing process steps is *prima facie* obvious in the absence of new or unexpected results. *In re Burhans* 154 F.2d 690, 69 USPQ 330 (CCPA 1946).

9. Regarding claims 87-88, Inoue and Houston disclose the sidewall is completely removed (Fig. 11-14). Hence, the burying film is located higher in level than that of the sidewall. Furthermore, Inoue and Houston disclose removing the protection film by a wet etch process which has an etching ratio higher than that of the burying film since the burying film remains after the etching process while the protection film is removed (col 8, lines 36-42; col 7, lines 5-9).

10. Regarding claims 89 and 91, Inoue and Houston disclose that the opening portion exposes the element isolation without removing the upper part of the semiconductor substrate (Fig. 1).

11. Regarding claims 90 and 92, Inoue and Houston disclose that the sidewall is not formed on the side face of the semiconductor substrate (Houston: Fig. 3).

12. Claim 81 is rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue et al. (U.S. 2003/0127667 A1; hereinafter 'Inoue') as modified by Houston (U.S. 6,096,612) as applied to claim 70 above, and further in view of Gardner et al. (U.S. 6,433,400 B1; hereinafter 'Gardner').

13. Regarding claim 81, Inoue and Houston disclose the method steps of claim 70 and that the photoelectric conversion section and the active region include an n-type impurity (Inoue: [0008]) but do not disclose implanting a p-type into a-side face portion of the trench in the semiconductor substrate. However, Gardner discloses implanting a p-type into a side face portion of the trench in the semiconductor substrate by using the protection film and the sidewall as a mask after the step of forming a trench and before the step of oxidizing the lateral sides of the trench (col 5, lines 42-52; Fig. 5-8). The motivation of performing this step is to create a channel stop, which decreases the effective width of the active areas. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Inoue and Houston with implanting a p-type impurity, as taught by Gardner, so as to create a channel stop layer.

Response to Arguments

14. Applicant's arguments with respect to claims 70, 77, 81, 83, and 87-92 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to REEMA PATEL whose telephone number is (571)270-1436. The examiner can normally be reached on M-F, 8:00-4:30 ET.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Garber can be reached on (571)272-2194. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Reema Patel/
Examiner, Art Unit 2812
8/28/08

/Charles D. Garber/
Supervisory Patent Examiner, Art Unit 2812